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Current Sense Amplifiers for Embedded SRAM in High-Performance System-on-a-Chip Designs

Springer Science & Business Media System-on-a-chip (SoC) designs result in a wide range of high-complexity, high-value semiconductor products. As the technology scales towards smaller feature sizes and chips grow larger, a speed limitation arises due to an in creased RC delay associated with interconnection wires. Innovative circuit techniques are required to achieve the speed needed for high-performance signal processing. Current sensing is considered as a promising circuit class since it is inherently faster than conventional voltage sense amplifiers. How ever, especially in SRAM, current sensing has rarely been used so far. Practi cal implementations are challenging because they require sophisticated analog circuit techniques in a digital environment. The objective of this book is to provide a systematic and comprehen sive insight into current sensing techniques. Both theoretical and practical aspects are covered. Design guidelines are derived by systematic analysis of different circuit principles. Innovative concepts like compensation of the bit line multiplexer and auto-power-down will be explained based on theory and experimental results. The material will be interesting for design engineers in industry as well as researchers who want to learn about and apply current sensing techniques. The focus is on embedded SRAM but the material presented can be adapted to single-chip SRAM and to any other current-providing memory type as well. This includes emerging memory technologies like magnetic RAM (MRAM) and Ovonic Unified Memory (OUM). Moreover, it is also applicable to array like structures such as CMOS camera chips and to circuits for signal trans mission along highly capacitive busses.

VLSI Design and Test

17th International Symposium, VDAT 2013, Jaipur, India, July 27-30, 2013, Proceedings

Springer This book constitutes the refereed proceedings of the 17th International Symposium on VLSI Design and Test, VDAT 2013, held in Jaipur, India, in July 2013. The 44 papers presented were carefully reviewed and selected from 162 submissions. The papers discuss the frontiers of design and test of VLSI components, circuits and systems. They are organized in topical sections on VLSI design, testing and verification, embedded systems, emerging technology.

Comparators in Nanometer CMOS Technology

Springer This book covers the complete spectrum of the fundamentals of clocked, regenerative comparators, their state-of-the-art, advanced CMOS technologies, innovative comparators inclusive circuit aspects, their characterization and properties. Starting from the basics of comparators and the transistor characteristics in nanometer CMOS, seven high-performance comparators developed by the authors in 120nm and 65nm CMOS are described extensively. Methods and measurement circuits for the characterization of advanced comparators are introduced. A synthesis of the largely differing aspects of demands on modern comparators and the properties of devices being available in nanometer CMOS, which are posed by the so-called nanometer hell of physics, is accomplished. The book summarizes the state of the art in integrated comparators. Advanced measurement circuits for characterization will be introduced as well as the method of characterization by bit-error analysis usually being used for characterization of optical receivers. The book is compact, and the graphical quality of the illustrations is outstanding. This book is written for engineers and researchers in industry as well as scientists and Ph.D students at universities. It is also recommendable to graduate students specializing on nanoelectronics and microelectronics or circuit design.

Integrated Hybrid Resonant DCDC Converters

Springer Nature This book provides a comprehensive, single-source on resonant switched-capacitor converters. It is written in the style of a handbook, with systematic guidelines, and includes implementation examples. The authors explore integrated hybrid resonant DCDC converters in order to achieve highly compact, energy efficient and cost-effective power management solutions in the growing fields of wearables and internet-of-things applications. They provide an introduction into hybrid converters as a new and promising converter class, which merges capacitive and inductive conversion concepts into one. Coverage ranges from fundamentals to implementation details, including topics such as power stage design, gate drive schemes, different control mechanisms for resonant operation and integrated passives. Introduces a new, multi-ratio resonant converter architecture, which enables lower switching frequencies and better passive component utilization; Discusses circuit block design for high efficiency of the power stage; Explores implementation details and concepts for integrated passives; Derives models, implements and compares to each other different control mechanisms.

VLSI Memory Chip Design

Springer Science & Business Media A systematic description of microelectronic device design. Topics range from the basics to low-power and ultralow-voltage designs, subthreshold current reduction, memory subsystem designs for modern DRAMs, and various on-chip supply-voltage conversion techniques. It also covers process and device issues as well as design issues relating to systems, circuits, devices and processes, such as signal-to-noise and redundancy.

Artificial Intelligence and Algorithms in Intelligent Systems

Proceedings of 7th Computer Science On-line Conference 2018, Volume 2

Springer This book presents the latest trends and approaches in artificial intelligence research and its application to intelligent systems. It discusses hybridization of algorithms, new trends in neural networks, optimisation algorithms and real-life issues related to the application of artificial methods. The book constitutes the second volume of the refereed proceedings of the Artificial Intelligence and Algorithms in Intelligent Systems of the 7th Computer Science On-line Conference 2018 (CSOC 2018), held online in April 2018.

Security and Privacy-Preserving Techniques in Wireless Robotics

CRC Press The wide gap between the existing security solutions and the actual practical deployment in smart manufacturing, smart home, and remote environments (with respect to wireless robotics) is one of the major reasons why we require novel strategies, mechanisms, architectures, and frameworks. Furthermore, it is also important to access and understand the different level of vulnerabilities and attack vectors in Wireless Sensor Network (WSN) and Wireless Robotics. This book includes an in-depth explanation of a secure and dependable Wireless Robotics (WR) architecture, to ensure confidentiality, authenticity, and availability. Features Blockchain technology for securing data at end/server side Emerging technologies/networking, like Cloud, Edge, Fog, etc., for communicating and storing data (securely). Various open issues, challenges faced in this era towards wireless robotics, including several future research directions for the future. Several real world's case studies are included Chapters on ethical concerns and privacy laws, i.e., laws for service providers Security and privacy challenges in wireless sensor networks and wireless robotics The book is especially useful for academic researchers, undergraduate students, postgraduate students, and industry researchers and professionals.

Introduction to VLSI Systems

A Logic, Circuit, and System Perspective

CRC Press With the advance of semiconductors and ubiquitous computing, the use of system-on-a-chip (SoC) has become an essential technique to reduce product cost. With this progress and continuous reduction of feature sizes, and the development of very large-scale integration (VLSI) circuits, addressing the harder problems requires fundamental understanding of circuit and layout design issues. Furthermore, engineers can often develop their physical intuition to estimate the behavior of circuits rapidly without relying predominantly on computer-aided design (CAD) tools. Introduction to VLSI Systems: A Logic, Circuit, and System Perspective addresses the need for teaching such a topic in terms of a logic, circuit, and system design perspective. To achieve the above-mentioned goals, this classroom-tested book focuses on: Implementing a digital system as a full-custom integrated circuit Switch logic design and useful paradigms that may apply to various static and dynamic logic families The fabrication and layout designs of complementary metal-oxide-semiconductor (CMOS) VLSI Important issues of modern CMOS processes, including deep submicron devices, circuit optimization, interconnect modeling and optimization, signal integrity, power integrity, clocking and timing, power dissipation, and electrostatic discharge (ESD) Introduction to VLSI Systems builds an understanding of integrated circuits from the bottom up, paying much attention to logic circuit, layout, and system designs. Armed with these tools, readers can not only comprehensively understand the features and limitations of modern VLSI technologies, but also have enough background to adapt to this ever-changing field.

IEICE Transactions on Electronics

Electronic Devices and Circuit Design

Challenges and Applications in the Internet of Things

CRC Press This new volume offers a broad view of the challenges of electronic devices and circuits for IoT applications. The book presents the basic concepts and fundamentals behind new low power, high-speed efficient devices, circuits, and systems in addition to CMOS. It provides an understanding of new materials to improve device performance with smaller dimensions and lower costs. It also looks at the new methodologies to enhance system performance and provides key parameters for exploring the devices and circuit performance based on smart applications. The chapters delve into myriad aspects of circuit design, including MOSFET structures depending on their low power applications for IoT-enabled systems, advanced sensor design and fabrication using MEMS, indirect bootstrap techniques, efficient CMOS comparators, various encryption-decryption algorithms, IoT video forensics applications, microstrip patch antennas in embedded IoT applications, real-time object detection using sound, IOT and nanotechnologies based wireless sensors, and much more.

Low-power, Low-voltage SRAM Circuits Design for Nanometric CMOS Technologies

Embedded SRAM memory is a vital component in modern SoCs. More than 80% of the System-on-Chip (SoC) die area is often occupied by SRAM arrays. As such, system reliability and yield is largely governed by the SRAM's performance and robustness. The aggressive scaling trend in CMOS device minimum feature size, coupled with the growing demand in high-capacity memory integration, has imposed the use of minimal size devices to realize a memory bitcell. The smallest 6T SRAM bitcell to date occupies a 0.1um2 in silicon area. SRAM bitcells continue to benefit from an aggressive scaling trend in CMOS technologies. Unfortunately, other system components, such as interconnects, experience a slower scaling trend. This has resulted in dramatic deterioration in a cell's ability to drive a heavily-loaded interconnects. Moreover, the growing fluctuation in device properties due to Process, Voltage, and Temperature (PVT) variations has added more uncertainty to SRAM operation. Thus ensuring the ability of a miniaturized cell to drive heavily-loaded bitlines and to generate adequate voltage swing is becoming challenging. A large percentage of state-of-the-art SoC system failures are attributed to the inability of SRAM cells to generate the targeted bitline voltage swing within a given access time. The use of read-assist mechanisms and current mode sense amplifiers are the two key strategies used to surmount bitline loading effects. On the other hand, new bitcell topologies and cell supply voltage management are used to overcome fluctuations in device properties. In this research we tackled conventional 6T SRAM bitcell limited drivability by introducing new integrated voltage sensing schemes and current-mode sense amplifiers. The proposed schemes feature a read-assist mechanism. The proposed schemes' functionality and superiority over existing schemes are verified using transient and statistical SPICE simulations. Post-layout extracted views of the devices are used for realistic simulation results. Low-voltage operated SRAM reliability and yield enhancement is investigated and a wordline boost technique is proposed as a means to manage the cell's WL operating voltage. The proposed wordline driver design shows a significant improvement in reliability and yield in a 400-mV 6T SRAM cell. The proposed wordline driver design exploit the cell's Dynamic Noise Margin (DNM), therefore boost peak level and boost decay rate programmability features are added. SPICE transient and statistical simulations are used to verify the proposed design's functionality. Finally, at a bitcell-level, we proposed a new five-transistor (5T) SRAM bitcell which shows competitive performance and reliability figures of merit compared to the conventional 6T bitcell. The functionality of the proposed cell is verified by post-layout SPICE simulations. The proposed bitcell topology is designed, implemented and fabricated in a standard ST CMOS 65nm technology process. A 1.2_ 1.2 mm2 multi-design project test chip consisting of four 32-Kbit (256-row x 128-column) SRAM macros with the required peripheral and timing control units is fabricated. Two of the designed SRAM macros are dedicated for this work, namely, a 32-Kbit 5T macro and a 32-Kbit 6T macro which is used as a comparison reference. Other macros belong to other projects and are not discussed in this document.

IEICE Transactions on Communications, Electronics, Information, and Systems

Asian Test Symposium

Index to IEEE Publications

Digital MOS Integrated Circuits II

With Applications to Processors and Memory Design

Piscataway, N.J. : IEEE Press Representing today's key research work in Digital MOS Integrated Circuits, this book provides you with the most comprehensive up-to-date guide to the latest information on a field that has witnessed phenomenal advances during the past ten years. Of great value to MOS digital circuits and systems designers as well as researchers, Digital MOS Integrated Circuits II covers the most recent developments in Digital MOS ICs and their applications in memory, signal and data processing, and application-specific ICs.

Science Abstracts

Electrical & electronics abstracts. Series B

A New Built-in Current Sensor for I[subscript DDT] Testing and Its Evaluation for Testing Open Defects in SRAMs

ABSTRACT: In very deep submicron technologies, supply current testing techniques are essential to achieve high fault coverage and to reduce test length. Due to high supply leakage currents, the quiescent power supply current (IDDQ) testing technique is no longer applicable for deep submicron technologies. However, the transient power supply current (IDDT) testing technique can be used in an environment of high leakage current and offers high fault coverage and reduced test time. A new built-in current sensor is presented here that has the potential to overcome some of the limitations of the other current sensors proposed previously. The current sensor can find application for testing embedded static random access memories (SRAMs) at high frequencies. It employs a high pass filter circuit to eliminate the effects of leakage current and utilizes cascaded high bandwidth amplifiers for high IDDT measurement sensitivity. Open defects in SRAMs are modeled as resistive open defects and studied using the new built-in current sensor for a 0.35 [(mu symbol)m] process technology. The current sensor efficiently detects the open defects in SRAMs that cause transition faults and destructive read-out faults. A two-vector test pattern is suggested with the current sensor for the detection of these faults. The first test vector is used to initialize the SRAM memory cell being tested, and the second test vector is applied to activate the fault.

Nanoelectronic Mixed-Signal System Design

McGraw Hill Professional Covering both the classical and emerging nanoelectronic technologies being used in mixed-signal design, this book addresses digital, analog, and memory components. Winner of the Association of American Publishers' 2016 PROSE Award in the Textbook/Physical Sciences & Mathematics category. Nanoelectronic Mixed-Signal System Design offers professionals and students a unified perspective on the science, engineering, and technology behind nanoelectronics system design. Written by the director of the NanoSystem Design Laboratory at the University of North Texas, this comprehensive guide provides a large-scale picture of the design and manufacturing aspects of nanoelectronic-based systems. It features dual coverage of mixed-signal circuit and system design, rather than just digital or analog-only. Key topics such as process variations, power dissipation, and security aspects of electronic system design are discussed. Top-down analysis of all stages--from design to manufacturing Coverage of current and developing nanoelectronic technologies--not just nano-CMOS Describes the basics of nanoelectronic technology and the structure of popular electronic systems Reveals the techniques required for design excellence and manufacturability

Proceedings of the ... Custom Integrated Circuits Conference

Proceedings of the IEEE 1987 Custom Integrated Circuits Conference

The Portland Hilton, Portland, Oregon ; Educational Sessions, the Westin Benson ; May 4-7, 1987

Deutsche Nationalbibliographie und Bibliographie der im Ausland erschienenen deutschsprachigen Veröffentlichungen

Hochschulschriften. Monatliches Verzeichnis. Reihe H

Proceedings

German books in print

CMOS Digital Integrated Circuits

Analysis and Design

The fourth edition of CMOS Digital Integrated Circuits: Analysis and Design continues the well-established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design, as well as addressing state-of-the-art technology issues highlighted by the widespread use of nanometer-scale CMOS technologies. In this latest edition, virtually all chapters have been re-written, the transistor model equations and device parameters have been revised to reflect the sigificant changes that must be taken into account for new technology generations, and the material has been reinforced with up-to-date examples. The broad-ranging coverage of this textbook starts with the fundamentals of CMOS process technology, and continues with MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, arithmetic building blocks, clock and I/O circuits, low power design techniques, design for manufacturability and design for testability.

IBM Journal of Research and Development

Low Energy Memory Design

EDN

Balancing Computation and Memory in High Capacity Reconfigurable Arrays

Embedded Memory Design for Multi-Core and Systems on Chip

Springer Science & Business Media This book describes the various tradeoffs systems designers face when designing embedded memory. Readers designing multi-core systems and systems on chip will benefit from the discussion of different topics from memory architecture, array organization, circuit design techniques and design for test. The presentation enables a multi-disciplinary approach to chip design, which bridges the gap between the architecture level and circuit level, in order to address yield, reliability and power-related issues for embedded memory.

Embedded Flash Memory for Embedded Systems: Technology, Design for Sub-systems, and Innovations

Springer This book provides a comprehensive introduction to embedded flash memory, describing the history, current status, and future projections for technology, circuits, and systems applications. The authors describe current main-stream embedded flash technologies from floating-gate 1Tr, floating-gate with split-gate (1.5Tr), and 1Tr/1.5Tr SONOS flash technologies and their successful creation of various applications. Comparisons of these embedded flash technologies and future projections are also provided. The authors demonstrate a variety of embedded applications for auto-motive, smart-IC cards, and low-power, representing the leading-edge technology developments for eFlash. The discussion also includes insights into future prospects of application-driven non-volatile memory technology in the era of smart advanced automotive system, such as ADAS (Advanced Driver Assistance System) and IoE (Internet of Everything). Trials on technology convergence and future prospects of embedded non-volatile memory in the new memory hierarchy are also described. Introduces the history of embedded flash memory technology for micro-controller products and how embedded flash innovations developed; Includes comprehensive and detailed descriptions of current main-stream embedded flash memory technologies, sub-system designs and applications; Explains why embedded flash memory requirements are different from those of stand-alone flash memory and how to achieve specific goals with technology development and circuit designs; Describes a mature and stable floating-gate 1Tr cell technology imported from stand-alone flash memory products - that then introduces embedded-specific split-gate memory cell technologies based on floating-gate storage structure and charge-trapping SONOS technology and their eFlash sub-system designs; Describes automotive and smart-IC card applications requirements and achievements in advanced eFlash beyond 4 0nm node.

Ageing of Integrated Circuits

Causes, Effects and Mitigation Techniques

Springer This book provides comprehensive coverage of the latest research into integrated circuits' ageing, explaining the causes of this phenomenon, describing its effects on electronic systems, and providing mitigation techniques to build ageing-resilient circuits.

Low-Power Digital VLSI Design

Circuits and Systems

Springer Science & Business Media Low-Power Digital VLSI Design: Circuits and Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized. The book also provides an extensive study of advanced CMOS subsystem design. A low-power design methodology is presented with various power minimization techniques at the circuit, logic, architecture and algorithm levels. Features: Low-voltage CMOS device modeling, technology files, design rules Switching activity concept, low-power guidelines to engineering practice Pass-transistor logic families Power dissipation of I/O circuits Multi- and low-VT CMOS logic, static power reduction circuit techniques State of the art design of low-voltage BiCMOS and CMOS circuits Low-power techniques in CMOS SRAMS and DRAMS Low-power on-chip voltage down converter design Numerous advanced CMOS subsystems (e.g. adders, multipliers, data path, memories, regular structures, phase-locked loops) with several design options trading power, delay and area Low-power design methodology, power estimation techniques Power reduction techniques at the logic, architecture and algorithm levels More than 190 circuits explained at the transistor level.

Embedded Computing and Mechatronics with the PIC32 Microcontroller

Newnes For the first time in a single reference, this book provides the beginner with a coherent and logical introduction to the hardware and software of the PIC32, bringing together key material from the PIC32 Reference Manual, Data Sheets, XC32 C Compiler User's Guide, Assembler and Linker Guide, MIPS32 CPU manuals, and Harmony documentation. This book also trains you to use the Microchip documentation, allowing better life-long learning of the PIC32. The philosophy is to get you started quickly, but to emphasize fundamentals and to eliminate "magic steps" that prevent a deep understanding of how the software you write connects to the hardware. Applications focus on mechatronics: microcontroller-controlled electromechanical systems incorporating sensors and actuators. To support a learn-by-doing approach, you can follow the examples throughout the book using the sample code and your PIC32 development board. The exercises at the end of each chapter help you put your new skills to practice. Coverage includes: A practical introduction to the C programming language Getting up and running quickly with the PIC32 An exploration of the hardware architecture of the PIC32 and differences among PIC32 families Fundamentals of embedded computing with the PIC32, including the build process, time- and memory-efficient programming, and interrupts A peripheral reference, with extensive sample code covering digital input and output, counter/timers, PWM, analog input, input capture, watchdog timer, and communication by the parallel master port, SPI, I2C, CAN, USB, and UART An introduction to the Microchip Harmony programming framework Essential topics in mechatronics, including interfacing sensors to the PIC32, digital signal processing, theory of operation and control of brushed DC motors, motor sizing and gearing, and other actuators such as stepper motors, RC servos, and brushless DC motors For more information on the book, and to download free sample code, please visit http://www.nu32.org Extensive, freely downloadable sample code for the NU32 development board incorporating the PIC32MX795F512H microcontroller Free online instructional videos to support many of the chapters

Robust SRAM Designs and Analysis

Springer Science & Business Media This book provides a guide to Static Random Access Memory (SRAM) bitcell design and analysis to meet the nano-regime challenges for CMOS devices and emerging devices, such as Tunnel FETs. Since process variability is an ongoing challenge in large memory arrays, this book highlights the most popular SRAM bitcell topologies (benchmark circuits) that mitigate variability, along with exhaustive analysis. Experimental simulation setups are also included, which cover nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis. Emphasis is placed throughout the book on the various trade-offs for achieving a best SRAM bitcell design. Provides a complete and concise introduction to SRAM bitcell design and analysis; Offers techniques to face nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis; Includes simulation set-ups for extracting different design metrics for CMOS technology and emerging devices; Emphasizes different trade-offs for achieving the best possible SRAM bitcell design.

Seventh Biennial IEEE Nonvolatile Memory Technology Conference

Proceedings : 1998 Conference : June 22-24, 1998, Albuquerque, NM, USA

Institute of Electrical & Electronics Engineers(IEEE) The mission of the IEEE International Nonvolatile Memory Technology Conference is to promote communication between nonvolatile memory technologists & systems developers worldwide. Its scope includes both very small & very large storage systems, & all classes of implementation technologies: semiconductor, optical, ferroelectric, & magnetic. Partial Contents: Semiconductor & Ferroelectric NVM; Magnetic NVM; Advanced Data Storage technology; Advanced Memory Technology; Packaging Controllers, & Systems

Proceedings, International Test Conference 1997

FPGA Architecture

Survey and Challenges

Now Publishers Inc FPGA Architecture: Survey and Challenges reviews the historical development of programmable logic devices, the fundamental programming technologies that the programmability is built on, and then describes the basic understandings gleaned from research on architectures. It is an invaluable reference for engineers and computer scientists. It is also an excellent primer for senior or graduate-level students in electrical engineering or computer science.

Nanometer Variation-Tolerant SRAM

Circuits and Statistical Design for Yield

Springer Science & Business Media Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques; Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view; Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.

Low-Power CMOS Wireless Communications

A Wideband CDMA System Design

Springer Science & Business Media Low-Power CMOS Wireless Communications: A Wideband CDMA System Design focuses on the issues behind the development of a high-bandwidth, silicon complementary metal-oxide silicon (CMOS) low-power transceiver system for mobile RF wireless data communications. In the design of any RF communications system, three distinct factors must be considered: the propagation environment in question, the multiplexing and modulation of user data streams, and the complexity of hardware required to implement the desired link. None of these can be allowed to dominate. Coupling between system design and implementation is the key to simultaneously achieving high bandwidth and low power and is emphasized throughout the book. The material presented in Low-Power CMOS Wireless Communications: A Wideband CDMA System Design is the result of broadband wireless systems research done at the University of California, Berkeley. The wireless development was motivated by a much larger collaborative effort known as the Infopad Project, which was centered on developing a mobile information terminal for multimedia content - a wireless `network computer'. The desire for mobility, combined with the need to support potentially hundreds of users simultaneously accessing full-motion digital video, demanded a wireless solution that was of far lower power and higher data rate than could be provided by existing systems. That solution is the topic of this book: a case study of not only wireless systems designs, but also the implementation of such a link, down to the analog and digital circuit level.

Embedded Memories for Nano-Scale VLSIs

Springer Science & Business Media Kevin Zhang Advancement of semiconductor technology has driven the rapid growth of very large scale integrated (VLSI) systems for increasingly broad applications, incl- ing high-end and mobile computing, consumer electronics such as 3D gaming, multi-function or smart phone, and various set-top players and ubiquitous sensor and medical devices. To meet the increasing demand for higher performance and lower power consumption in many different system applications, it is often required to have a large amount of on-die or embedded memory to support the need of data bandwidth in a system. The varieties of embedded memory in a given system have alsobecome increasingly more complex, ranging fromstatictodynamic and volatile to nonvolatile. Among embedded memories, six-transistor (6T)-based static random access memory (SRAM) continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. But as the technology scaling continues, SRAM design is facing severe challenge in mainta- ing suf?cient cell stability margin under relentless area scaling. Meanwhile, rapid expansion in mobile application, including new emerging application in sensor and medical devices, requires far more aggressive voltage scaling to meet very str- gent power constraint. Many innovative circuit topologies and techniques have been extensively explored in recent years to address these challenges.